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[Parallel and Scientific Computing Laboratory](#)

[Department of Communication Engineering](#)

[National Chiao Tung University](#)

1001 Ta Hsueh Road, HsinChu City 300,
TAIWAN

CHENG-KAI CHEN

RESEARCH INTEREST

Evolutionary Computation: With an emphasis on evolutionary optimizations for Electronic Design Automation (EDA), and the development of an optimization framework for defining general problems and solvers.

Data Visualization: Visi - Multi-dimensional data visualizer.

Semiconductor Device Simulation: By using adaptive finite volume method to perform semiconductor device simulations; quantum corrections for nanoscale device simulations; analysis for dopant fluctuation.

Parallel and Distributed Computation: Using Message-Passing Interface (M.P.I.) for semiconductor device simulation and evolutionary computation; Parallelization for 2D/3D device simulation; Domain decomposition and I-V point parallelization; Parallelization for time-dependent high frequency circuit simulation; Distributed evolutionary system.

Computational Geometry: One-irregular mesh generation. (for semiconductor device simulation); Polygon overlap problem, point location problem. (for Optical proximity correction and Conformal mapping in printed circuit board resistance-capacitance analysis)

Programming Language: A cross-platform system library; C/C++/C# programming techniques.

RESEARCH EXPERIENCE

Jan. 2003 - Present : *Research Assistant*

Served my military service as a research assistant of Professor Yiming Li. (*Parallel and Scientific Computing Laboratory at Department of Communication Engineering*)

Jan. 2001 - July 2002 : *Graduate Student*

Under advisory of Professor Chuen-Tsai Sun and Professor Yiming Li, I focus my attention to the use of evolutionary techniques to solve high dimensional problem on electronic design automation.

RESEARCH ACTIVITY

[Application Development]

1. [UOF - Unified Optimization Framework](#). (2005~present). contributors: **Cheng-Kai Chen**, Yen-Yu Cho, Yiming Li (director)
2. [Visi - Multi-dimensional Data Visualizer](#). (2005~2006). contributors: **Cheng-Kai Chen**, Yiming Li (director)
3. [ExtractCAD - Device Compact Model Parameter Optimization Tool](#). (2003~2005). contributors: Yiming Li, **Cheng-Kai Chen**, Yen-Yu Cho, Pu Chen, Chuan-Sheng Wang, Shao-Ming Yu.
4. [CPSL - Cross-Platform System Library](#). (2004~2005). contributors: **Cheng-Kai Chen**, Victor Liu, Dannis Lin.

[Research Project]

1. An evolutionary optimization for Electronic Design Automation (EDA). (2003~present). contributors: Yiming Li, **Cheng-Kai Chen**, Chuan-Sheng Wang, Yen-Yu Cho, Shao-Ming Yu.
2. [Semiconductor device simulation](#):
 - Solve Drift-Diffusion and Hydrodynamic models for MOSFET, DT-MOS, PN-Diode, Double-Gate MOSFET, SOI, Surrounding Gate MOSFET, TFT. (2002~2006). contributors: Yiming Li, **Cheng-Kai Chen**, Pu Chen.
 - Adaptive Finite Volume Method for Solving Poisson Equation with One-irregular Mesh. [\[Link\]](#)
 - [Parallelization to speedup the simulation process](#). (2003~2006). contributors: **Cheng-Kai Chen**, Pu Chen, Yiming Li (director)
 - Quantum corrections for nanoscale device simulations. (2003~2005). contributors: Yiming Li, **Cheng-Kai Chen**, Shao-Ming Yu.
 - Statistical analysis for MOSFET implement dopant fluctuation. (2006~present). contributors: Yiming Li, **Cheng-Kai Chen**, Shao-Ming Yu.
3. [Distributed evolutionary system](#). (2004~2006). contributors: **Cheng-Kai Chen**, Yiming Li (director)
4. [Genome Alignment Parallelization](#). (2005). contributors: **Cheng-Kai Chen**, Yiming Li (director)
5. [Parallelization for time-dependent high frequency circuit simulation](#). (2002). contributors: **Cheng-Kai Chen**, Kuen-Yu Huang, Yiming Li (director)
6. Computational Geometry
 - One-irregular mesh generation. (2001~2003). contributors: Yiming Li, **Cheng-Kai Chen**.
 - Polygon overlap problem, point location problem- for Optical proximity correction and [Conformal mapping in printed circuit board resistance-capacitance analysis](#). (2005~2006). contributors: Yiming Li, **Cheng-Kai Chen**, Yen-Yu Cho.

EDUCATION

Jan. 2001 - July 2002

Master of Science in Computer and Information Science
College of Computer Science

National Chiao Tung University, Hsinchu City, Taiwan

Thesis: A Genetic Algorithm for Deep-Submicron MOSFET Parameters Extraction and Simulation

Advisor: Professor Chuen-Tsai Sun, Professor Yiming Li

Graduate GPA (All): 3.76/4.00

Graduate GPA (Tech Courses): 3.87/4.00

Sep. 1997 - Jan. 2001

Bachelor of Science in Computer and Information Science

Department of Computer Science

National Chiao Tung University, Hsinchu City, Taiwan

Graduate GPA (All): 3.69/4.00

Graduate GPA (Tech Courses): 3.88/4.00

TEACHING EXPERIENCE

Mar. 2002] June. 2002

Graduate Teaching Assistant

National Chiao Tung University, Hsinchu City, Taiwan

Graduate course: Computer Aided Network Design And Analysis

Instructor: Professor Fung-Yuel Chang

Graded homework and examinations, developed the course term project, and helped students in office hours.

Sep. 2001] Jan. 2002

Graduate Teaching Assistant

National Chiao Tung University, Hsinchu City, Taiwan

Graduate course: Computer-aided Circuit Analysis

Instructor: Professor Fung-Yuel Chang

Graded homework and examinations, developed the course term project, and helped students in office hours.

THESIS

A Genetic Algorithm for Deep-Submicron MOSFET Parameters Extraction and Simulation

Genetic algorithm is a stochastic-based optimization strategy with its randomly but systematically search strategy which is usually applied for solving complex problem, such as simulated model parameters extraction. To characterize the properties of MOSFET accurately, various compact models have been proposed for deep-submicron and nanoscale MOSFET device simulation. Each model consists of diverse governing equations and parameters. It leads to a multivariable optimization problem to be solved and extracted efficiently for the device applications.

Different approaches, for instance the direct method and numerical method have been applied to extract and optimize the model parameters. In this work we present a unified multi-objective evolutionary approach for BSIM3 MOSFET model parameter extraction. In contrast to conventional time-consuming large-scale approach, our genetic algorithm includes: (1) a physical-based weight function; (2) floating-point operators; and (3) dynamic mutation techniques, and solves the problem efficiently. The proposed method outputs a set of optimal parameters for device simulation; in our simulation experiences, this method is stable and accurate.

Comprehensive comparisons among models are reported for the parameters sensitivity test. Simulations and measurements for sub-micron MOSFETs compact models are examined to show the accuracy and robustness of the method. The developed CAD tool can be further applied to extract nanoscale MOSFETs parameters for advanced VLSI circuit design and SOC applications.

ACADEMIC ACTIVITY

[Summer school]

June 2004

Attend to "2004 Summer School on Computational Materials Science-Introduction to Computational Nanotechnology" at the University of Illinois at Urbana-Champaign, U.S.A. [[Link](#), [Photos](#)]

[Conference]

July. 2006

Attend to "Genetic and Evolutionary Computation Conference (GECCO 2006)" in Seattle, WA, U.S.A. [[Link](#), [Photos](#)]

Paper Poster of the following paper:

"A Unified Optimization Framework for Microelectronics Industry."

Sep. 2005

Participate in "Solid State Devices and Materials (SSDM 2005)" in Kobe, Japan [[Link](#), [Photos](#)]

May 2005

Participate in "International Conference on Computer Science (ICCS 2005)" at Emory University, Atlanta, U.S.A. [[Link](#), [Photos](#)]

June 2002

Attend to "Sixth International Conference on Neural Networks and Soft Computing (IEEE ICNNSC 2002)" in Zakopane, Poland [[Link](#), [Photos](#)]

Oral Speaker of the following paper:

"A floating-point based evolutionary algorithm for model parameters extraction and optimization in HBT device simulation."

April 2001

Attend to "International Parallel and Distributed Symposium (IPDPS 2001)" in San Francisco, U.S.A.

Oral Speaker of the following paper:

"An Implementation of Parallel Dynamic Load Balancing for Adaptive Computing in VLSI Device Simulation."

ACADEMIC PUBLICATION

Selected Journal papers and Book articles (Total 7 papers, selected 5 papers)

1. Y. Li and **Cheng-Kai Chen**, "Visi - A VTK- and QT-Based Open-Source Project for Data Visualization," submitted for publication in ***IEEE Transactions on Visualization and Computer Graphics***, Nov. 2006. [PDF\(1563K, 8 pages\)](#), [project link](#).
2. Y. Li and **Cheng-Kai Chen**, "A Simulation-Based Evolutionary Technique for Inverse Doping Profile Problem of Sub-65 nm CMOS Devices," accepted for publication in ***Journal of Computational Electronics***, Dec. 2006. [PDF\(354K, 6 pages\)](#), [citation](#).
3. Y. Li and **Cheng-Kai Chen**, "A Distributed-Simulation-Based Computational Intelligence Algorithm for Nanoscale Semiconductor Device Inverse Problem," ***Lecture Notes in Computer Science***, Vol. LNCS 4331, Nov. 2006, pp. 231-240. [PDF\(273K, 10 pages\)](#), [citation](#).
4. Y. Li and **Cheng-Kai Chen**, "Parallelization of Multiple Genome Alignment," ***Lecture Notes in Computer Science***, Vol. LNCS 3726, Sep. 2005, pp. 910-915. [PDF\(428K, 6 pages\)](#), [citation](#), [project link](#).
5. Y. Li, **Cheng-Kai Chen**, and S.-M Yu, "A Two-Dimensional Thin-Film Transistor Simulation Using Adaptive Computing Algorithm", in "Lecture Series on Computer and Computational Sciences I," Edited by T. Simos and G. Maroulis, ***Brill Academic Publishers***, ISBN: 90-6764-418-8, Boston, November 2004, pp. 586-588. [PDF\(206K, 4 pages\)](#).

Selected Conference and Workshop papers (Total 8 papers, selected 5 papers)

1. Y. Li, S.-M Yu, and **Cheng-Kai Chen**, "A Coupled Simulation and Optimization Approach to Nanodevice Fabrication with Minimization of Electrical Characteristics Fluctuation," Accepted by *The 6th IEEE Conference on Nanotechnology (IEEE-NANO 2006)*, Cincinnati, Ohio, U.S.A., July 16-20, 2006. [PDF\(360K, 4pages\)](#), [citation](#).
2. Y. Li, **Cheng-Kai Chen**, and Y.-Yu Cho, "A Unified Optimization Framework for Microelectronics Industry," Accepted by *ACM Genetic and Evolutionary Computation Conference 2006 (ACM GECCO 2006)*, Seattle, Washington, USA, 8-12 July, 2006, pp. 1875-1876, ISBN: 1-59593-186-4. [PDF\(77K, 2 pages\)](#), [citation](#), [project link](#).
3. Y. Li, C.-T Sun, and **Cheng-Kai Chen**, "A Floating-Point Based Evolutionary Algorithm for Model Parameters Extraction and Optimization in HBT Device Simulation," Accepted by *IEEE The Sixth International Conference on Neural Networks and Soft Computing (IEEE ICNNSC 2002)*, Zakopane, Poland, 11-15 June, 2002.
4. Y. Li, K.-Y Huang, **Cheng-Kai Chen**, Chien-Ping Lee, "A Parallel Computational Technique for High Frequency HBT Circuit Simulation", *Technical Proceedings of 5th ACR/IEEE/SIAM International Conference on Modeling and Simulation of Microsystems (MSM 2002)*, Puerto Rico, 22-25 April, 2002, pp. 376-379. [PDF \(277K, 4 pages\)](#), [citation](#).
5. Y. Li, **Cheng-Kai Chen**, S.-S Lin, T.-S Chao, J.-L Liu, and Simon M. S, "An Implementation of Parallel Dynamic Load Balancing for Adaptive Computing in VLSI Device Simulation", *Proceedings of The 15th IEEE/ACM International Parallel and Distributed Processing Symposium (IEEE/ACM IPDPS 2001)*, San Francisco, April 2001, pp. 17.3.1-17.3.6. [PDF \(562K, 6 pages\)](#), [citation](#), [project link](#).

Technical reports

1. **Cheng-Kai Chen**. (2006). *Adaptive Finite Volume Method for Solving Poisson Equation with One-irregular Mesh*. (unpublished draft) [PDF \(676K, 14 pages, in Traditional Chinese\)](#), [PDF \(606K, 14 pages, in English\)](#).

Thesis

1. **Cheng-Kai Chen**. (2002). *A Genetic Algorithm for Deep-Submicron MOSFET Parameters Extraction and Simulation*. Master's thesis, National Chiao Tung University, Hsinchu, Taiwan. [PDF \(701K, 119 pages\)](#), [PDF of thesis orals \(1069K, 59 pages\)](#).

Published books (for intermediate level)

1. **Cheng-Kai Chen**, Yen-Liang Lin. (2002). *C# Programming*. Taipei, Taiwan: Key Hold Information CO., Ltd. ISBN: 986-7844-09-2. (in Traditional Chinese) [Link](#)
2. **Cheng-Kai Chen**, Jin-Hui Chen. (2001). *The Essential of C++ Library*. Taipei, Taiwan: Key Hold Information CO., Ltd. ISBN:957-2011-21-9. (in Traditional Chinese) [Link](#)
3. **Cheng-Kai Chen**, Jin-Hui Chen. (2001). *The Essential of C++ Library*. Beijing, China: China Railway Publishing House. ISBN:711-3044-33-6. (in Simplified Chinese) [Link](#)
4. **Cheng-Kai Chen**, Jin-Hui Chen. (2001). *Introduction and Application of C/C++ Language*. Taipei, Taiwan: Acore Publishing CO., Ltd. ISBN:957-2005-14-6. (in Traditional Chinese) [Link](#)

[PDF](#)

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